REMARKS

This is in response to the Office Action dated January 30, 2006. Claims 1-10 and 13-19 are pending. Reexamination and reconsideration are respectfully requested.

The Office Action indicates that claims 1, 13 and 14 are allowed and the Office Action rejects claims 2, 5-10 and 13-16. The Office Action objects to claims 3 and 4 "as being dependent upon a rejected base claim." Applicant submits that the office action improperly objects to claims 3 and 4, because claims 3 and 4 depend from allowed claim 1. Applicant requests correction of this apparent error and an unambiguous indication that claims 3 and 4 are allowed.

The Office Action rejects claims 2, 5-10 and 13-16 as anticipated by U.S. Patent No. 6,384,621 to Gibbs, et al. Applicant submits that the claims of the present application distinguish over the Gibbs patent and are in condition for allowance.

The Office Action specifically references FIGS. 1 and 5 of the Gibbs patent. FIGS. 1 and 5a of the Gibbs patent, as well as the rest of the Gibbs patent, show only a single unit circuit connected to the output. Consequently, the Gibbs patent does not anticipate independent claims 2, 13 and 15, each of which requires multiple unit circuits where each of the unit circuits has a pull up transistor connected to a common node and a pull down transistor connected to a common node.

The Office Action has identified in the Gibb patent a single unit circuit connected to one output terminal. This is true of both FIG. 1 and FIG. 5 in the Gibb patent. This is the conventional configuration where there is one unit circuit for each output terminal. There are not multiple common nodes within corresponding multiple unit circuits, with the multiple common nodes all connected to a single

output terminal. The Office Action errs when it references plural common nodes in FIG. 1 of the Gibb patent that are connected to one output terminal. FIG. 1 and FIG. 5 of the Gibb patent unambiguously show a single unit circuit connected to a single output terminal and, implicitly, a number of unit circuits each connected to a single corresponding one of the output terminals of the device.

The present application describes a number of input and output circuits that can implement the JEDEC standard input and output characteristics described in the application. Claim 2 relates for example to the circuit illustrated in FIG. 3, which includes first and second unit circuits B1 and B2, each including a pull-up transistor (TP1 and TP2, respectively) and a pull-down transistor (TN1 and TN2, respectively) and each having a common node (C1 and C2, respectively) between their respective pull-up and pull-down transistors and connected through resistors (R11 and R12, respectively) to a single output terminal (OUT). Because two unit circuits are provided with distinct resistors between the unit circuits and the output terminal, output current variations are reduced and there is greater flexibility in designing the performance of the FIG. 3 circuit.

In addition, the two resistors provided along the output current path further limit variations on the output current of the circuit. This is discussed for the FIG. 3 circuit at page 15, lines 1-8 of the present application. Claim 2 reflects this aspect of the disclosure by reciting, "first resistors formed respectively between said common nodes of said plurality of unit circuits and said common connecting point."

Applicant submits that claim 2 distinguishes over the Gibb patent by reciting the presence of a plurality of unit circuits, as defined by claim 2, with the common nodes of the plurality of unit circuits connected to the single output terminal through first and second resistors. This is not true of the Gibb patent. For example, there are not multiple resistors connected to a single output terminal in

the FIG. 1 embodiment of the Gibb patent. Rather, there is a single resistor connected to a single output terminal. Consequently claim 2 distinguishes over the Gibb patent by reciting, "first resistors formed respectively between said common nodes of said plurality of unit circuits and said common connecting point."

The circuit of FIG. 5a of the Gibb patent includes a plurality of impedance elements like that illustrated in FIG. 5b, all connected in parallel. Pull up transistors 206 and connected to respective resistors 204 and the respective resistors 204 are connected to a common node. Pull down transistors 210 connect to respective resistors 208 and the respective resistors are connected to the single common node. For the FIG. 5b version of the FIG. 5a circuit, there are no resistors connected between the common node and the output terminal (DOUT PIN 108). The FIG. 5C portion of the FIG. 5a circuitry does not use resistors and so there are no resistors connected between the common node and the output terminal (DOUT PIN 108). Consequently, none of the FIG. 5 implementations of the Gibb patent's circuitry meet claim 2's recitation of "first resistors formed respectively between said common nodes of said plurality of unit circuits and said common connecting point."

The resistor shown in prior art FIG. 1 of the Gibb patent is not used in the FIG. 5 embodiment of the Gibb patent. Consequently, the Office Action's reference to resistor 18 of FIG. 1 is misplaced, as that resistor is not used in the embodiments of the Gibb patent.

Consequently, claim 2 and its dependent claims distinguish over the Gibb patent by reciting "first resistors formed respectively between said common nodes of said plurality of unit circuits and said common connecting point" and are in condition for allowance.

Independent claim 13 recites "a plurality of unit circuits ... each" including "a pull up transistor controlled by a first input signal ... and a pull-down transistor controlled by a second input signal ...." What is illustrated in FIG. 5A and FIG. 5B is a single unit circuit from the perspective of claim 13 because all of the circuits 194 are connected in parallel and receive the same input signal from the drive 190. Consequently, claim 13 and its dependent claim 14 distinguish over the Gibb patent because the FIG. 5a circuit provides the same input signal to all of the pull up and pull down transistors of the Fig. 5a circuit. Claims 13 and 14 recite "a plurality of unit circuits ... each" including "a pull up transistor controlled by a first input signal ... and a pull-down transistor controlled by a second input signal ..." and so distinguish over the teachings of the Gibb patent.

Independent claim 15, in pertinent part, recites "first resistors connected respectively between said common nodes of said plurality of unit circuits and a common connecting point of said common nodes." This limitation distinguishes over the Gibb patent for the reasons discussed above with respect to claim 2. That is, the Gibb patent does not teach the use of resistors between the common nodes and common connecting points in a buffer circuit as defined by claim 15. As such, claim 15 and its dependent claims 16-19 distinguish over the art of record and are in condition for allowance.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (310) 785-4600 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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